IN THE CLAIMS:

Claim 1 (Currently Amended): A liquid crystal display panel, comprising:

a plurality of gate lines arranged along a first direction on a first substrate;

a plurality of data lines arranged along a second direction on the first substrate to cross the gate lines to define a plurality of unit pixels;

an insulating layer disposed over the gate and data lines;

a common electrode disposed on a second substrate opposite to the first substrate;

a plurality of pixel electrodes, each pixel electrode provided in each of the unit pixels partitioned by the gate line and the data line; and

a plurality of side electrodes overlapping the data lines along a length direction of the data lines, the side electrode in the pixel being extended to a neighboring pixel,

wherein the insulating layer is provided between the side electrode and the data lines and a width of the side electrode is greater than a width of the data lines.

Claim 2 (Original): The panel according to claim 1, further comprising a thin film transistor provided in the unit pixel.

Claim 3 (Original): The panel according to claim 1, wherein the pixel electrode and the side electrode are made of a same material.

Claim 4 (Original): The panel according to claim 3, wherein the common electrode and the side electrodes comprise transparent conductive material films.

Claim 5 (Original): The panel according to claim 1, wherein each of the side electrodes are provided between adjacent unit pixels.

Claim 6 (Original): The panel according to claim 1, wherein the insulating layer includes an organic material film.

Claim 7 (Original): The panel according to claim 6, wherein the insulating layer includes at least one of benzocyclobutene (BCB), spin-on-glass (SOG), and photo-acryl.

Claim 8 (Original): The panel according to claim 1, wherein the side electrodes overlap the gate lines with at least the insulating layer therebetween.

Claim 9 (Original): The panel according to claim 1, wherein the pixel electrode is divided into a first region and a second region and the first and second regions are electrically interconnected by a connection region.

Claim 10 (Currently Amended): A liquid crystal display panel, comprising:

a plurality of gate lines formed on a first substrate;

a first insulating layer and an active layer formed on the first substrate;

a plurality of data lines formed on a surface of the active layer;

a second insulating layer formed on another surface of the active layer upon which the data lines are formed;

a plurality of side electrodes formed on a surface of the second insulating layer to overlap the data lines along a length direction of the data lines, the side electrode in the pixel being extended to a neighboring pixel; and

a plurality of pixel electrodes formed on surfaces of the second insulating layer separated from the side electrodes,

wherein a width of the side electrode is greater than a width of the data lines.

Claim 11 (Original): The panel according to claim 10, wherein the first insulating layer is a gate insulating layer separating a gate electrode from the active layer.

Claim 12 (Original): The panel according to claim 10, wherein the second insulating layer includes an organic material layer.

Claim 13 (Original): The panel according to claim 10, further comprising:

a second substrate bonded to the first substrate;

a liquid crystal material layer formed between the first and second substrates;

a black matrix formed on a surface of the second substrate aligned to the gate lines and the data lines;

a color filter layer formed on the second substrate aligned with the unit pixel;

a common electrode formed on another surface of the second substrate upon which the black matrix and the color filter layer are formed; and

an electric field partition formed on the second substrate.

Claim 14 (Original): The panel according to claim 13, further comprising a liquid crystal material layer formed between the first and second substrates.

Claim 15 (Original): The panel according to claim 14, wherein the liquid crystal material layer has negative dielectric anisotropy.

Claim 16 (Original): The panel according to claim 13, wherein the electric field partition is a rib formed on a surface of the common electrode.

Claim 17 (Original): The panel according to claim 13, wherein the electric field partition is a slit formed between adjacent portions of the common electrode.

Claim 18 (Original): The panel according to claim 10, further comprising a plurality of partitions formed on the first substrate between adjacent ones of the plurality of pixel electrodes.

Claim 19 (Currently Amended): A method for fabricating a liquid crystal display panel, comprising:

forming a plurality of gate lines, a plurality of data lines, and a plurality of thin film transistors on a first substrate;

forming a passivation layer on a surface of the first substrate upon which the gate lines, the data lines, and the thin film transistors are formed;

forming a transparent conductive material on a surface of the passivation layer;

forming a plurality of side electrodes extending along a length direction of the data lines and overlapping the data lines by patterning the transparent conductive material, the side electrode in the pixel being extended to a neighboring pixel;

forming a plurality of pixel electrodes separated from the side electrodes by patterning the transparent conductive material;

forming a black matrix, a color filter, and a common electrode on a second substrate;

forming an electric field partition on the common electrode;

bonding the first and second substrates together aligning the pixel electrodes to the common electrode; and

forming a liquid crystal material layer between the bonded first and second substrates,

wherein a width of the side electrode is greater than a width of the data lines.

Claim 20 (Original): The method according to claim 19, wherein the transparent conductive material includes at least one of indium tin oxide (ITO) an indium zinc oxide (IZO).

Claim 21 (Original): The method according to claim 19, further comprising etching the passivation layer to expose drain electrode portions of the thin film transistors.

Claim 22 (Original): The method according to claim 19, wherein the forming of an electric field partition includes forming at least one rib on a surface of the common electrode.

Claim 23 (Original): The method according to claim 19, wherein the forming of an electric field partition includes forming at least one slit in the common electrode by etching a part of the common electrode.

Claim 24 (Original): The method according to claim 19, wherein the forming a plurality of side electrodes and the forming a plurality of pixel electrodes is performed simultaneously by the patterning of the transparent conductive material.